Real-Time Fault Detection Algorithm for Interior Permanent Magnet Synchronous Motor Drive using DSP/FPGA

Pracoviště: Regionální inovační centrum elektrotechniky
Číslo dokumentu: xxxxx
Typ zprávy: Výzkumná zpráva
Řešitelé: Serge Pacome Bosson
Vedoucí projektu: Zdeněk Peroutka
Počet stran: 37
Datum vydání: 20.6.2022
Oborové zařazení: 2.2 Electrical engineering, Electronic engineering, Information engineering - Electrical and electronic engineering

Zadavatel / zákazník:

Zpracovatel / dodavatel:
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This research as been supported by the project No. SGS-2021-021

Anotace

Klíčová slova

Detekce chyb vinutí, PMSM, FPGA, FFT,

Název zprávy v anglickém jazyce / Report title

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Anotace v anglickém jazyce / Abstract

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Klíčová slova v anglickém jazyce / Keywords

Interior permanent magnet synchronous motor, pulse-width modulated inverter, real-time fault detection, transient excitation, fast Fourier transform, hardware FFT processor, spectral analysis, digital signal processors, field programmable gate array

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List of symbols and shortcuts

GPS	Global Position System

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1 Introduction

Interior permanent magnet synchronous motors (IPMSM) are attractive for a variety of applications due to their high electromagnetic torque per permanent magnet volume, high efficiency, high power factor, and low noise [1]. The IPMSM drive is one of the integral parts of modern electric vehicles [2]. In the standard automotive industry, electric power steering systems are also developed with interior permanent-magnet (IPM) motors. However, IPM motors are subject to a wide variety of abnormal operations, including faults. These faults pose particular problems due to the presence of rotating rotor magnets that cannot be turned off during faults. Therefore, it is important to understand the responses of an IPM motor to any potential fault condition to prevent fault-induced damage to the drive system. In such a system, continuous operation is required, so a failure of the IPMSM drive is unacceptable.

For these reasons, some research on fault detection and diagnosis for IPMSM drives has been conducted. Liu et al. [3] investigated the fluctuation of high-frequency *d*-axis inductance by analysing the current spectrum to distinguish the rotor demagnetization and eccentricity faults of the IPM motor. Welchko et al. [4] have presented a modified d–q axis model for the analysis of single phasing in IPM motor drives. The effect of magnetic saturation has been considered in the model. The performances of the model have not been investigated for symmetric and asymmetric short circuit faults. Jiangbiao He et al. [5] proposed three diagnostics approaches, namely, the stator current spectrum analysis, the negative sequence components method, and the space-vector pendulous oscillation method to detect stator winding short-circuit fault in IPM motor drives. Myoungho Kim et al. [6] proposed a turn-fault detection method for inverter-fed Interior Permanent Magnet Synchronous Machines using high-frequency current injection when the motor is at standstill. The proposed detection method injects the high-frequency current into the stator windings with three directions successively and examines the generated loss of each case. Byunghwan Lee et al [7] proposed the model-based fault detection and identification (FDI) algorithm of current sensor for the IPMSM based on parity equation approach. In order to consider the modelling errors during the transient manoeuvres, the time varying adaptive threshold method was used. M. A. S. K. Khan et al [8] presented a method for classification and detection of disturbances including faults in the three-phase IPM motors. A rule classifier, which is based on the root mean square (RMS) comparison of the coefficients of 5^{th} level details and approximations of the line currents, has been developed in order to classify different faulted currents of a three-phase IPM motor. Zia Ullah et al [9] presented a torque angle-based inverter-embedded technique for the online detection and identification interturn short fault (ITSF) and partial irreversible demagnetization fault (PIDF) in an interior permanent magnet synchronous motor (IPMSM). Jiadong Lu et al [10] proposed a position sensor fault detection method using a single dc-bus current sensor with accuracy uncertainty in an IPMSM drive. In [11] is presented a comprehensive analysis of inter-turn-short fault (ITSF) in a fractional slot concentrated winding (FSCW) interior permanent magnet synchronous motor (IPMSM). A. Khlaief et al [12] proposed a detection and localization of open-phase faults in IPMSM drives based on discrete Fourier transform phase. In this method the state space model of the PMSM is expressed in the d-q synchronous reference to study the phenomena occurred in the stator current. Min Zhu et al [13] used the torque ripple for online demagnetization fault diagnosis in IPMSM drive using continuous wavelet transforms (CWT) and grey system theory (GST). A fault diagnostics and protection scheme

for the interior permanent-magnet (IPM) synchronous motors using wavelet packet transform (WPT) and artificial neural network is proposed in [14]. In the proposed technique, the line currents of different faulted and normal conditions of the IPM motor are pre-processed by the WPT then WPT coefficients of line currents are used as inputs of a three-layer feedforward neural network. An online diagnostics of the uniform and partial irreversible demagnetization fault (IDF) in interior permanent magnet synchronous motor (IPMSM) using the frequency spectrum of the input-voltage is presented in [15]. Bochao Du et al [16] used digital signal processor for real-time interturn short-circuit fault diagnosis strategy for the interior permanent-magnet synchronous motor (IPMSM) of an electric vehicle (EV). In this method, online and offline detection were integrated into the diagnostic strategy to optimize diagnostic performance based on work cycle of an EV. Gilbert Hock Beng Foo et al [17] used an extended Kalman filter for sensor fault detection and isolation in IPMSM drives. The filter is used to simultaneously estimate the phase currents and rotor speed of the IPM machine. These signals are compared with the corresponding sensor signals, and the faulty sensor is identified based on a fault detection logic. P. Castro Palavicino et al [18] proposed a method to detect and diagnose an inter-turn short circuit in an interior permanent magnet synchronous machine by using a current observer to estimate a specific disturbance related to the fault. This disturbance is defined as a fault index current. S.-C. Yang et al [19] used pulsating-type voltage injection for stator winding fault detection in interior permanent-magnet (PM) machines. The pulsating voltage is superimposed on d-axis with respect to the rotor-referred synchronous frame, then winding fault reflected signals which occur in the injection induced current ripples is measured. Seokbae Moon et al [20] proposed an algorithm based on analysis of currents in the synchronous frame to detect and classify demagnetization and ITSF in IPMSMs. The algorithm is based on changes of magnitude and angle of currents in the synchronous frame.

A review of the state of the art in the field of fault detection in IPMSM drives leads us to conclude that, despite all the existing work done by several authors regarding diagnostics methods for IPMSM drives, there is very little research regarding the development of drive system diagnostics that are, to some extent, independent of the motor control algorithm, in order to provide an "independent" diagnostics capability. In addition to this requirement, real-time fault detection algorithms must take into account other requirements such as no sensitivity to machine speed, torque load and machine parameters.

Taking into account all these considerations, this paper proposes a new algorithm to detect faults in IPMSM drive for an embedded application. The drive system diagnostics includes three main module:

- An intelligent controller within the DSP, allowing a measurement and control unit to work in conjunction with the motor control for on-line parameter estimation.
- A floating point FFT processor within the FPGA, for real-time harmonics analysis, operating independently of the motor control.
- A decision making model within the FPGA, to distinguish healthy and faulty states of the motor.

The rest of the paper is organized as follows. Section II gives the theoretical core for transient leakage inductance estimation used for feature extraction for condition indicator identification. Section III presents the proposed real-time fault detection algorithm. Section IV presents the experimental results with an open phase fault. Finally, this paper ends up with concluding remarks and perspective extensions in Section V.

2 Fault feature extraction for identifying condition indicators

To design an algorithm to detect or predict faults, we use condition indicators extracted from some parameters or system data to design a decision making model that analyse data in real time to distinguish healthy and faulty states of the machine or to determine the current state. Condition indicators can be derived from data using signal-based condition indicators such as time domain, frequency domain and time-frequency domain.

2.1 Estimation of the transient leakage inductance

Wolbank et al. [21] proposed a method of detection of faults in induction motor drives using only the current sensors that already present in the control system and exploiting the switching transient of the voltage source inverter. The main idea is to exploit the machine response to transient excitation. Short voltage pulses applied by inverter switching to machine terminals will evoke a current response which is dominated by the transient leakage inductance.

The machines electrical behaviour is described with the well-known stator equation in space phasor representation:

$$\underline{v_s} = r_s . \underline{i_s} + l_l . \frac{di_s}{dt} + \frac{d\lambda_r}{dt} \quad (1)$$

Obviously, the applied voltage phasor $\underline{v_s}$, generated by any of the active switching states of the inverter, leads to a transient current change $\frac{di_s}{dt}$. The actual inverter switching state, the dc-link voltage, the value of the leakage inductance l_l, and the stator-resistance voltage drop $r_s . \underline{i_s}$, as well as the time derivative of the rotor flux $\frac{d\lambda_r}{dt}$ (back electromotive force (EMF)), they all influence this current change.

The stator resistance and the back EMF, will act as a disturbance when identifying the transient reactance.

If two subsequent pulses whose voltage phasors point in opposite spatial directions are applied, the fundamental-wave operating point of the machine is almost unchanged due to the symmetrical nature of the excitation, as can be seen in Fig. 1. The figure shows a symmetrical pulse sequence consisting of positive and negative switching states of one phase (e.g., −V, +V, −V, +V) and the resulting time trace of a corresponding phase current. It is then possible to carry out the measurement (of the resulting current change Δi_I and Δi_{II}), which is symmetrical with respect to the fundamental-wave operating point, using the built-in current sensors of the inverter. The value of the fundamental-wave operating point is indicated by the horizontal time axis in Fig. 1. The switching states are indicated by the dashed lines, and the corresponding voltage phasors (V), the duration (Δτ) for taking the current samples, and the resulting current change (Δi) are marked in grey. The value of the dc-link voltage and the back EMF can be considered constant during the short periods, (some 10 µs) necessary to generate the pulse sequence and perform the measurement. As a result, it is possible to eliminate the influence of back EMF as well as that of the stator resistance using an excitation sequence consisting of two different switching states, as seen in Fig. 1. If the two measurement durations $\Delta\tau_I$ and $\Delta\tau_{II}$ are equal, the elimination is performed simply by taking the difference between the two results Δi_I and Δi_{II}. By combining the phase values of the current changes to one phasor, it is possible to obtain a

space phasor of the current difference. After elimination of the back EMF and the stator resistance, the relation between the voltage of the pulse sequence and the measured current change can then be rewritten according to (2). As a result, the inductance $l_{l,t}$ is the only remaining machine parameter. The value of the fundamental-wave leakage inductance l_l according to (1) differs from the transient leakage inductance responsible for the current change. It is denoted as transient leakage $l_{l,t}$ in the following:

$$\underline{v_{s,I}} - \underline{v_{s,II}} = l_{l,t} \cdot \left(\frac{\Delta \mathrm{i}_{sI}}{\Delta \tau} - \frac{\Delta \mathrm{i}_{sII}}{\Delta \tau}\right) = l_{l,t} \cdot \left(\frac{\Delta \mathrm{i}_{sI} - \Delta \mathrm{i}_{sII}}{\Delta \tau}\right) \tag{2}$$

If the machine is perfectly symmetrical as was assumed, the value of $l_{l,t}$ will be a scalar, and the direction of the resulting current slope is parallel to the overall pulse voltage. However, on every real machine, even if faultless, there are always some inherent spatial asymmetries, which also influence the phase values of the transient leakage. As a result, the direction of the applied pulse voltage and current slope will no longer be collinear. In (2), an asymmetry of the machine can be considered by introducing a complex value for the transient leakage $l_{l,t}$ that combines the asymmetry of the three phase values in one parameter. Using a two-axis representation, the magnitude of the transient leakage $|l_{l,t}|$ now becomes angle-dependent and can be described by an offset value l_{offset} and an angle-dependent modulation l_{mod}. Assuming only a single dominant asymmetry of the inductance and only taking into account its fundamental wave, the offset and modulation values can be described:

$$l_{offset} = \frac{l_{max} + l_{min}}{2} \tag{3}$$

$$\underline{l}_{mod} = \frac{l_{max} - l_{min}}{2} \cdot e^{2\gamma} = l_{mod} \cdot e^{2\gamma} \tag{4}$$

The so-introduced complex transient inductance $\underline{l}_{l,t}$ is composed of a scalar portion l_{offset} and a complex portion $\underline{l}_{mod}$. The “offset” part is representing the symmetrical portion of the asymmetrical machine, and the “mod” part is representing the modulation due to asymmetry. The magnitude and angle of $\underline{l}_{mod}$ contain the information about the asymmetry. l_{max} and l_{min} define the maximum and minimum values, respectively, of the transient inductance along the air gap. The angle γ of the modulation gives the spatial position of the maximum inductance within one pole pair. The asymmetry has a period of two with respect to the fundamental wave.

As shown in (2), it is sufficient to monitor the resulting current slope to calculate the complex transient inductance. By inversion with portion $\underline{y}_{l,t} = 1/\underline{l}_{l,t}$, the number of mathematical calculations is reduced, and the measurement-control system need not carry out divisions.

$$\left(\frac{\Delta \mathrm{i}_{sI} - \Delta \mathrm{i}_{sII}}{\Delta \tau}\right) = \underline{y}_{l,t} \cdot \underline{v}_{s,I-II} \tag{5}$$

The parameter $\underline{y}_{l,t}$ contains all the information regarding the asymmetry of the machine. This can be detected by solving (6); a simple calculation for a digital signal processor (DSPs) as the applied pulse sequence is known, and the phasor of the current difference $\Delta \mathrm{i}_s$ is obtained according to Fig. 1

$$\underline{y}_{l,t} = \frac{\left(\frac{\Delta \mathrm{i}_{sI} - \Delta \mathrm{i}_{sII}}{\Delta \tau}\right)}{\underline{v}_{s,I-II}} \tag{6}$$

As each of the voltage pulses has the same magnitude of 1 p.u., (dc-link voltage), the difference voltage phasor in the three main phases result to:

$$\underline{v}_{s,I-II,U} = \underline{v}_{s,U+} - \underline{v}_{s,U-} = 2e^{j0} \quad (7)$$

$$\underline{v}_{s,I-II,V} = \underline{v}_{s,V+} - \underline{v}_{s,V-} = 2\, e^{j2\pi/3} \quad (8)$$

$$\underline{v}_{s,I-II,W} = \underline{v}_{s,W+} - \underline{v}_{s,W-} = 2\, e^{j4\pi/3} \quad (9)$$

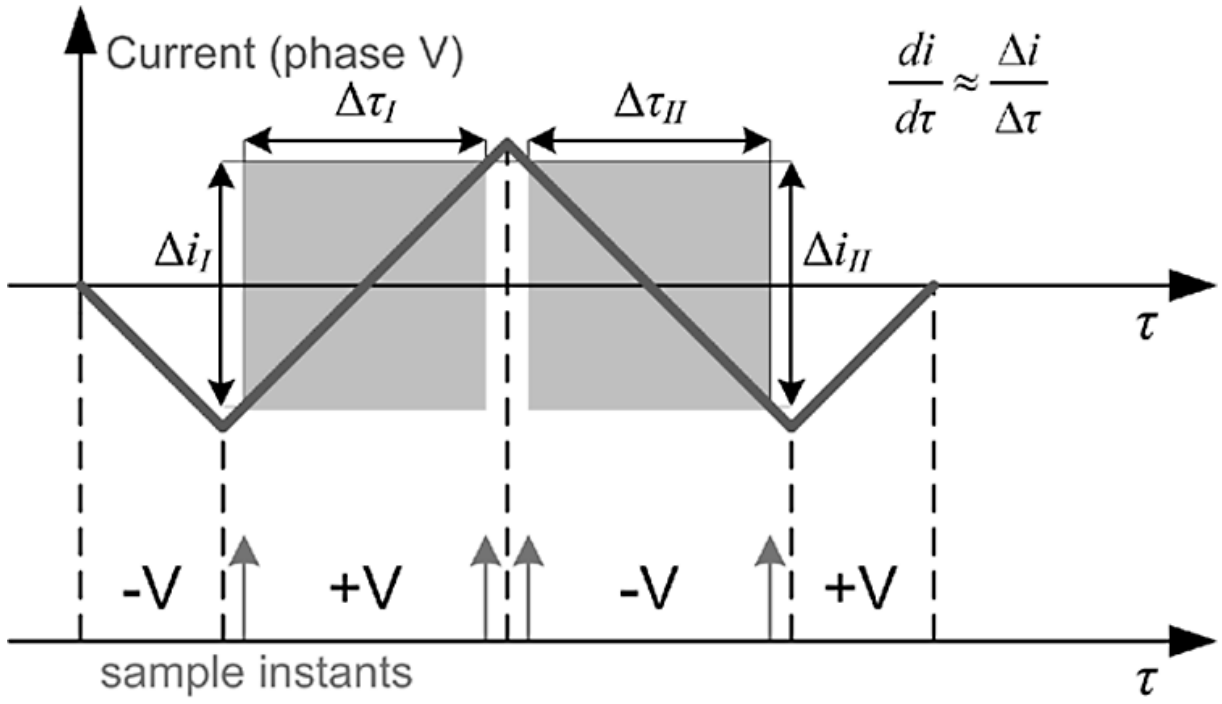

Fig. 1. Voltage pulses in phase U direction [21]

2.2 Feature extraction

In every machine, faultless or not, the symmetrical part in the current response signal is predominant. Usually, this part is responsible for about 90% of the overall resulting current change phasor, as presented in Fig. 2. Thus, it is clear that the symmetrical portion has to be eliminated to obtain a high sensitive fault indicator. The elimination can be done using a voltage excitation sequence that sequentially changes its resulting direction ($\underline{v}_{s,I-II,U}$, $\underline{v}_{s,I-II,V}$, $\underline{v}_{s,I-II,W}$) in the main three phase axes. Thus, three different current change phasors are obtained ($\underline{\Delta i}_{s,I-II,U}/\Delta\tau$, $\underline{\Delta i}_{s,I-II,V}/\Delta\tau$, $\underline{\Delta i}_{s,I-II,W}/\Delta\tau$), each with the symmetrical portion pointing in one main phase direction (see Fig. 2). Combining the current change phasors of each phase to one resulting phasor, the share of the symmetrical machine leads to a zero sequence and is eliminated (9).

The remaining phasor $\underline{Complex\_phasor}$ after carrying out this step now only contains information on machine asymmetries and will serve as fault feature extraction:

$$\underline{Complex\_phasor} = \frac{\underline{\Delta i}_{s,I-II,U}}{\Delta\tau} + \frac{\underline{\Delta i}_{s,I-II,V}}{\Delta\tau}.e^{-j2\pi/3} + \frac{\underline{\Delta i}_{s,I-II,W}}{\Delta\tau}.e^{j2\pi/3} \quad (10)$$

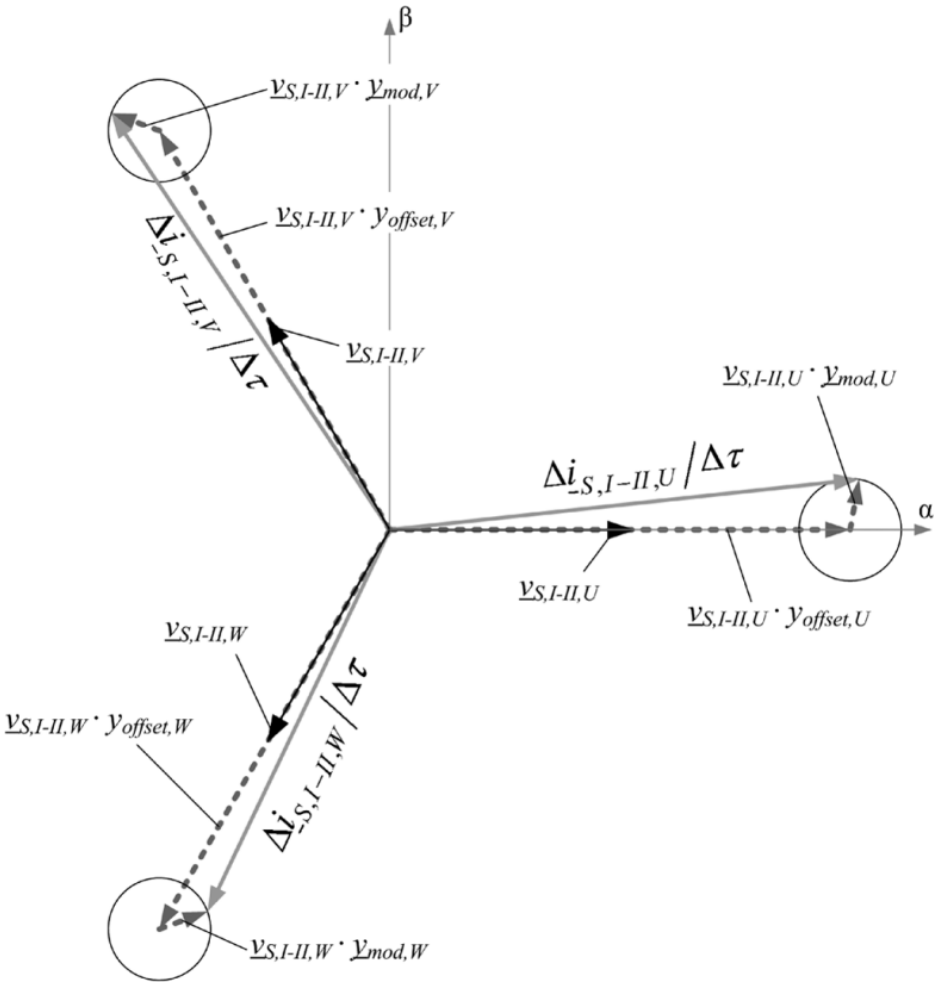

Fig.2. Relations of the symmetrical (90%) and the modulated (10%) portion corresponding to the voltage pulses in the main phases. The voltage phasors are clearly reduced to improve visibility [21]

2.3 Fault indicator based on spatial harmonic content of the complex phasor

The complex phasor serves as the base for the determination of the fault indicators. However, the complex phasor not only consists of fault-induced modulations but also contains some inherent asymmetries. In a real machine even faultless, there are always some inherent asymmetries present. These asymmetries are detectable and separable due to their deterministic behaviour leading to modulation of the complex phasor when the inherent asymmetries spatially move at a period of 2pi mechanical radians called spatial period. In synchronous electrical machines, there are four aspects that define the complex phasor's harmonic content; the permanent magnets, the stator currents, the winding distribution and the machine's geometry [22].

The fast Fourier transformation (FFT) provides an effective possibility to separate their modulations from the complex phasor signal in order to use the spatial harmonic contents in the complex phasor as condition indicators. It is however necessary to collect a set of complex phasors clearly showing the spatial movement of the different inherent modulations. This collection can be established by a specific measuring sequence as follows. In a first step the voltage pulse sequences are applied to all three main phase directions and by measurement of the current signal and subsequent signal processing the complex phasor is obtained as described above. In the next stage the rotor is moved, the data acquisition is repeated, and a complex phasor set for one mechanical period of the modulation is acquired.

3 Proposed real-time fault detection algorithm

Our goal is to design an intelligent control and diagnostics algorithm for electric drives which operates in real time and which is embedded into the drive system. The drive system diagnostics is intended for traction drives application so uses a combination of DSP and FPGA as is often the case in modern industrial drives. The requirement of the drive system diagnostics is that it has to operate independently of the motor control algorithm and other algorithm routines that running in real time during operation of the traction drive. The fault detection algorithm also must be not sensitive in machine parameters, speed, and load variations. Fig. 3. show the proposed drive system diagnostics. To satisfy the above requirements, it includes an intelligent controller designed as a finite state machine that allows a measurement and control unit to operate in conjunction with the field oriented control algorithm to extract the saliency of the machine during low speed operation. This parameter, as shown in the work of Goran Stojcic et al [23], contains all the information about the asymmetries of the machine and has been successfully used to detect any type of fault in induction motor drives. After estimating the fault feature parameter, a floating FFT

processor is designed for real-time harmonic identification for condition indicator extraction, which operates independently of the motor control. Finally, a decision making algorithm using a simple comparator is designed for fault detection.

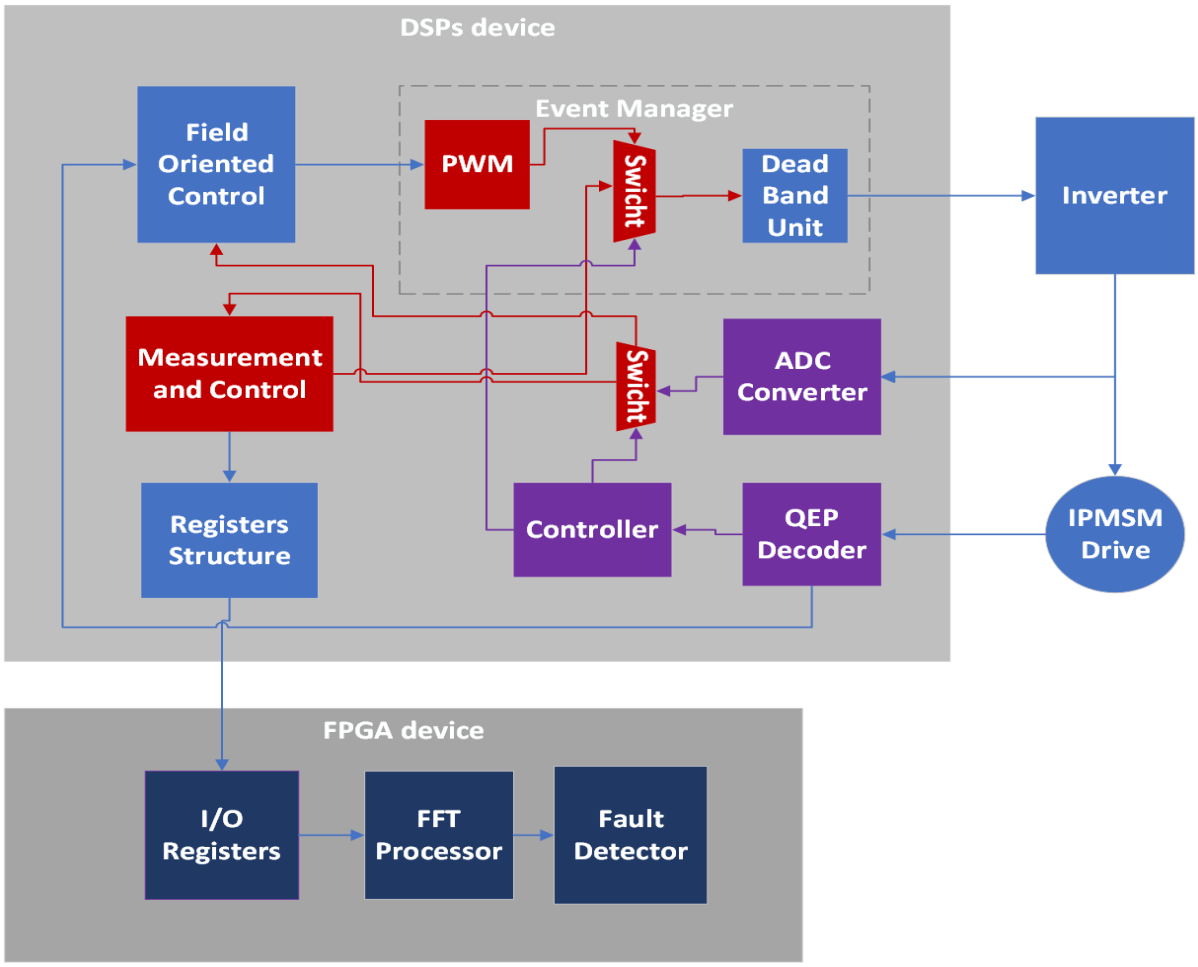

Fig.3. Proposed drive system diagnostics

3.1 Intelligent controller for saliency extraction

Fig. 4 shows the intelligent control algorithm implemented using DSP TMS320F28377S from Texas instruments, coded in C language with Code Composer Studio. The machine is fed by a full-size inverter and operated by a field-oriented control scheme. The inverter control scheme is a standard pulse width modulation (PWM). The controller decides when the fault feature has to be estimated. In a first step, the low speed operation of the machine is checked. When the motor operates at low speed, in the next step, a reference angle value is generated. This value is forwarded where there is compared with the actual rotor angle obtained from the field oriented control. When the rotor angle matches with the reference angle, the current controller and the PWM modulator are interrupted and a special voltage pattern is applied, and the measurement of the resulting current differences as shown in Fig. 1. The finite state machine controller sequentially changes the direction of the voltage

excitation in the three phase axes, so that three different current change phasors are obtained. Finally, a complex phasor is calculated according to (4). The estimated complex phasor now is transferred to FPGA for further signal processing. After that, a new reference angle value is generated. This procedure is repeated until a set of complex phasor values is obtained with respect to one mechanical revolution.

The measurement and control algorithm is depicted in Fig. 5. It contains three main interrupt routines. The timing of the whole estimation process algorithm is based on internal timer of the PWM modulator and it is set to 5 kHz (200μs).

The ePWM timer interrupt routine starts the voltage pulse generation in the specific phase direction and the corresponding current derivative measurement, according to the direction status fixed by the finite state machine controller. After that the CPU timer is triggered to start A/D oversampling start of conversion. Then the CPU timer interrupt routine interrupts the field oriented control algorithm and starts conversion of external A/D converter. After conversion end, direct memory transfer (DMA) is automatically started and data from A/D converter are transferred into internal RAM of MCU. When DMA transfer ends, second interrupt is executed. This function executes a circular buffer function to get oversampling data from external A/D converter. When the buffer is filled, the CPU timer is stopped in order to interrupt the oversampling A/D start of conversion, and the current derivatives are calculated by taking four sampling data according to the phase direction given by state machine status. After the complex phasor is computed and transferred to FPGA, new reference angle is generated. This procedure is repeated until a set of complex phasor values is obtained with respect to one mechanical revolution.

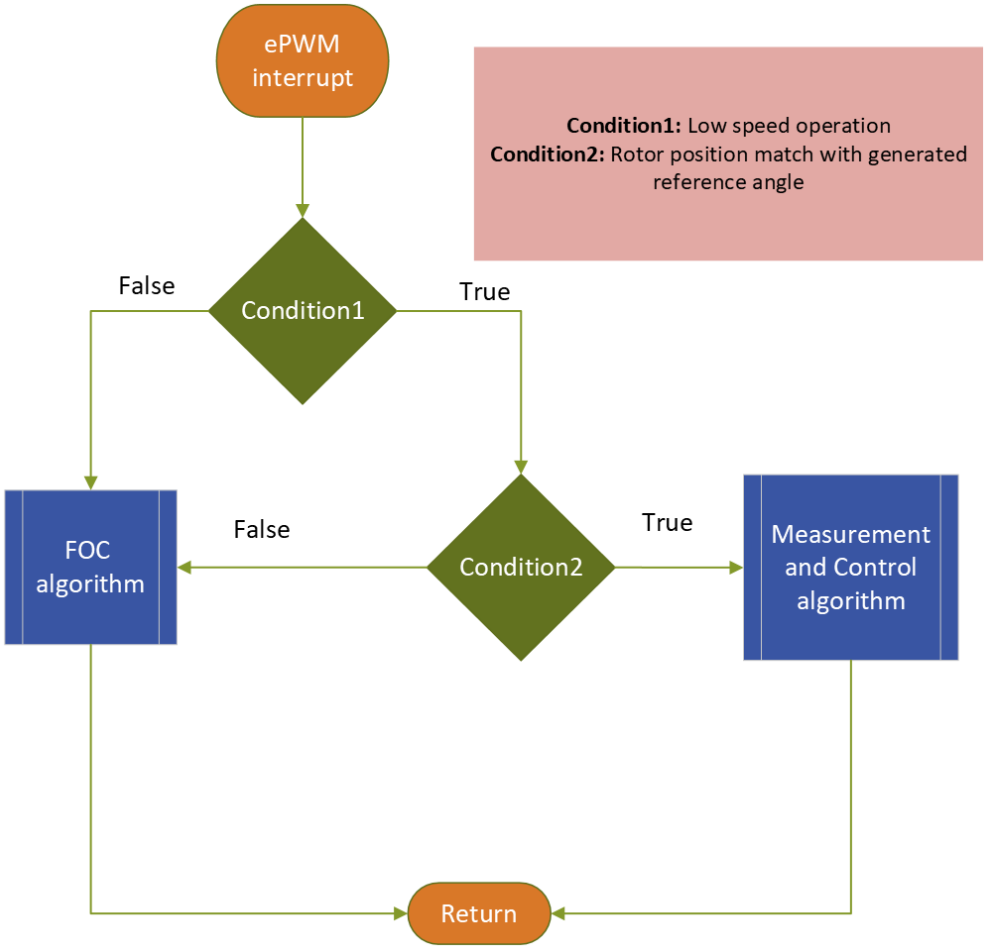

Fig.4. Smart controller algorithm

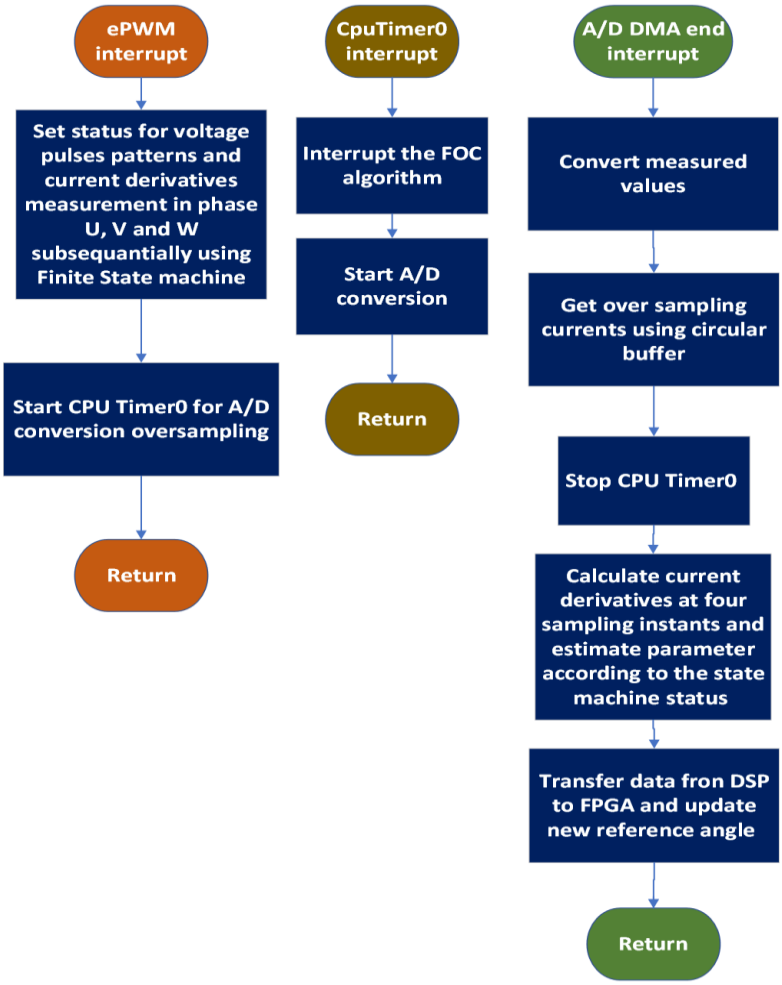

Fig.5. Measurement and control algorithm

3.2 Floating point FFT Processor

3.2.1 FFT algorithm

The discrete Fourier transform (DFT) X_k of an N-point discrete-time signal x_n is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n \, W_N^{nk} \text{ , } 0 < k < N-1 \quad (11)$$

$$W_N^{nk} = e^{-j2\pi nk/N} \quad (12)$$

Where the twiddle factor W_N^{nk} denotes the N-point primitive root of unity. Equation (11) shows that, in the case when x_n is a complex sequence, a complete direct evaluation of an N-point DFT requires $(N-1)^2$ complex multiplications and (N-1) complex additions. Thus for reasonably large of values of N (on the order of 1000), direct evaluation of the DFT requires an inordinate amount of computation. The most common algorithm for efficient computation of the DFT when N is power of two is the Fast Fourier Transform (FFT) algorithm proposed by Cooley and Tuckey [24]. The idea behind the FFT is to break the original N-point sequence into shorter sequences, the DFT's of which can be combined to give the DFT of the original sequence.

In our work, the Radix-2 Decimation in Time (DIT) Cooley-Tuckey algorithm is chosen for the FFT computation. We choose Radix-2 since it offers a simple butterfly structure and

simpler control. It can process any input sequence lengths which are powers of two. In the Radix-2 DIT FFT algorithm, N is divided by two in each stage, and butterfly-like operations are performed on two samples in each stage. The number of stages is given by, v = log_2N. The computational complexity of the DFT is reduced from O(N^2) to O(Nlog_2N.).

Fig. 6 shows the signal flow graph for a radix-2 8-point FFT algorithm using decimation in time. The input data sequence are stored in bit-reversed order. At each stage or processing element (PE), (N/2) butterfly operations are performed. The lower edges of the butterfly is multiplied by the appropriate twiddle factor which depends upon the stage number and the sample points. The lower output of the butterflies always have the transmittance -1. The outputs of the butterflies are then fed to the next stage.

The basic DIT algorithm of the FFT is given below.

Define two (N/2)-point sequences x_1(n) and x_2(n) as the even and odder member of x(n), respectively i.e.

x_1(n) = x(2n) 0 < n < (N/2)-1 (13)

x_2(n) = x(2n+1) 0 < n < (N/2)-1 (14)

The N-point DFT of x(n) can be written as

$$X(k) = \sum_{\substack{n=0 \\ n\ even}}^{N-1} x(n)\, W_N^{nk} + \sum_{\substack{n=0 \\ n\ odd}}^{N-1} x(n)\, W_N^{nk} \quad (15)$$

$$X(k) = \sum_{n=0}^{N/2-1} x_1(n)\ W_N^{2nk} + \sum_{n=0}^{N/2-1} x_2(n)\ W_N^{(2n+1)k} \quad (16)$$

Recognizing that W_N^2 can be written as

$$W_N^2 = e^{j(2\pi/N)2} = e^{j2\pi/(\frac{N}{2})} = W_{N/2} \quad (17)$$

Equation (16) can be put in the form

$$X(k) = \sum_{n=0}^{N/2-1} x_1(n)\ W_{N/2}^{nk} + W_N^k \sum_{n=0}^{N/2-1} x_2(n)\ W_{N/2}^{nk} \quad (18)$$

$$X(k) = X_1(k) + W_N^k X_2(k) \quad (19)$$

Where $X_1(k)$ and $X_2(k)$ are seen to be the (N/2)-point DFT of $x_1(n)$ and $x_2(n)$.

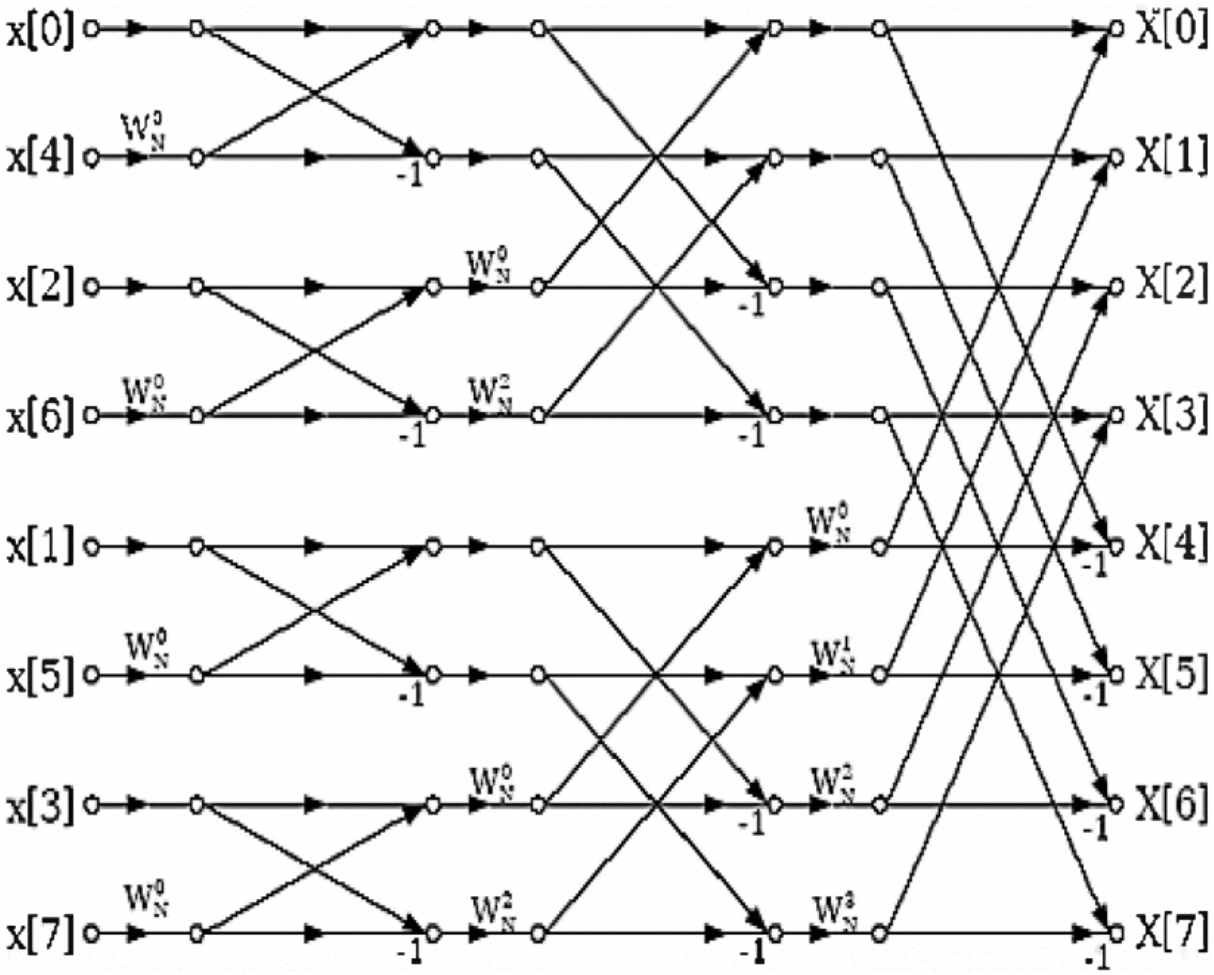

Fig. 6. Radix-2 DIT FFT signal-flow graph of length 8.

3.2.2 FFT processor architecture

FFT processor is a hardware implementation for FFT algorithm. This processor is widely used in many applications such as wireless sensor networks, medical imaging, geophysics and mechanical applications [25]. These applications require a low power, high speed and small area processor.

Generally, FFT architectures can be classified into memory-based and pipeline architecture styles [26]. Pipeline FFT is a class of parallel algorithms that contains an amount of parallelism equal to log_rN where N denotes the N-point DFT. Thus, for a radix-r pipeline FFT there will be (log_rN) separate hardware butterfly computations proceeding in parallel. Generally, the pipeline FFT processors have two popular design types. One uses a single-path delay feedback (SDF) pipeline architecture, and the other uses a multiple-path delay commutator (MDC) pipeline architecture. The multi-path delay commutator (MDC) FFT also known as feed-forward FFT scheme can achieve higher throughput rate by using multiple data paths, while the single-path delay feedback (SDF) FFT scheme needs less memory and hardware complexity with the delay feedback scheme. Memory-based architecture is widely adopted to design an FFT processor, also known as the single processing element (PE) approach. This design style is usually composed of a main PE and several memory units, thus the hardware cost and the power consumption are both lower than the other architecture style.

In this work, we use a ping-pong memory-based FFT to design the floating point FFT processor. The developed floating point FFT processor based on radix-2 DIT algorithm, is intended for embedded real-time high resolution motor monitoring. We implement a 256 point FFT in hardware using IEEE-754 single precision input data.

Fig. 7 shows the proposed hardware FFT processor implemented using FPGA Cyclone III EPC40 from Altera. There are five major building units in the proposed floating point FFT processor. These units are an address generation unit, two blocks of two-port RAM, a butterfly arithmetic unit, a twiddle factor ROM, and finally a controller.

The Address Generation Unit (AGU) controls the generation of addresses for reading and writing the memory contents to and from the Butterfly Processing Unit (BFU). The AGU also generates signals that control writes to memory as well as which memory bank is read.

The two blocks of two-port RAM perform “ping-pong” reads and writes scheme, and store the data we wish to transform and hold the intermediate values as we step through the FFT levels. All data busses shown represent complex data transfer (double bit widths to accommodate both real and imaginary values). We read from one RAM block, process through the BFU and write to the other RAM block.

The Butterfly Processing Unit (BFU) performs a special 2-point FFT on the data pairs specified by the AGU. The butterfly structure utilizes the parallel and pipeline structure to minimize delay caused by the FFT calculation [27]. Each butterfly requires four multiplication units (two for the real and two for the imaginary) and six addition units (three for the real and three for the imaginary). The atomic operation is schematically shown in Fig. 8. In this project we use the Altera floating point Megafunction to implement the floating point adder/subtractor and the floating point multiplier [28]. The MegaWizard Plug-In Manager of Quartus is used to create the design files which are then instantiated in the designed Butterfly Processing Unit.

The twiddle factor ROM contains the look-up table of real and imaginary values of the required “roots of unity” that are passed to the BFU.

The controller affects the efficiency of the floating point FFT processor. The goal of the controller is to provide the control signals to the different parts of the FFT processor. The proposed designed controller operates using finite state machine. Let us describe the action of the different building units managed by the controller. Memory 1 (the top block) is loaded with the data samples to be transformed (in bit-reversed address order) and the Start FFT signal is triggered. The FFT Done signal goes low and the AGU starts cycling through the Memory 1 addresses and the twiddle factor addresses as the BFU processing pipeline begins to fill. After a number of clock cycles, data begins to appear at the output of the BFU. The AGU begins to generate write cycles to Memory 2 (the bottom block) and the processed data is written to Memory 2. When the AGU reaches the end of the data buffer, the read address counter stops while the write address counter continues until the BFU pipeline has completely flushed out. Once the output data is completely written, the “level counter” increments and the read address counter and twiddle factor address counter begins to increment in an appropriately permuted order that depends on the level counter value. With this, the whole process repeats until the level counter indicates that we have completed the full transform. When this happens, the FfT Done signal is asserted, the BFU pipeline is flushed and the whole FFT processor goes into a wait state. The results of the transform can

now be read out and new data samples can be written into the memory. The Start FFT signal is triggered and the next batch of data is transformed.

To realize the hardware for algorithm, Quartus and ModelSim-Altera EDA tools where used to synthesize and simulate the design. In order to verify the functionality of the 256 floating point FFT processor, the VHDL code for the overall system was developed. We use Matlab as a standard model to generate a series of 256 floating point complex data and save these numbers in a certain file. The processor reads the numbers using ModelSim-Altera, and then performs FFT. The Matlab compares the results generated by VHDL with those generated by Matlab. The RTL synthesis view is shown in Fig. 9. From the Fig. 9, we can see that the total logic elements are used 38% and the total memory bits are occupied 32%. The saving use of logic elements meets the system requirement of rational utilization of FPGA resource.

Fig. 10 and Fig. 11 results illustrate respectively input data set and the final FFT results as they written to memory. The time taken by the FFT processor to complete one set of 256 floating point FFT is 16.376 micro seconds as shown in Fig. 11.

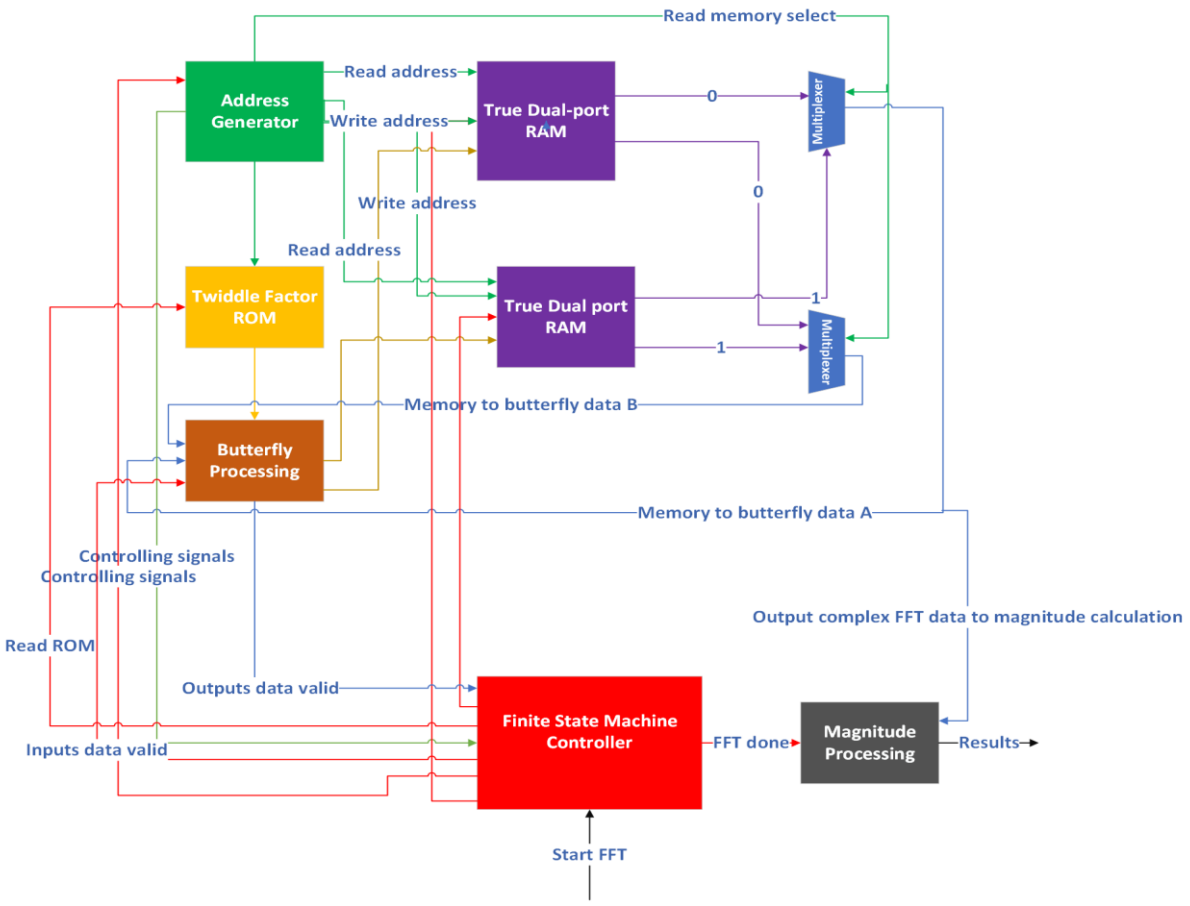

Fig.7. Hardware floating point FFT processor

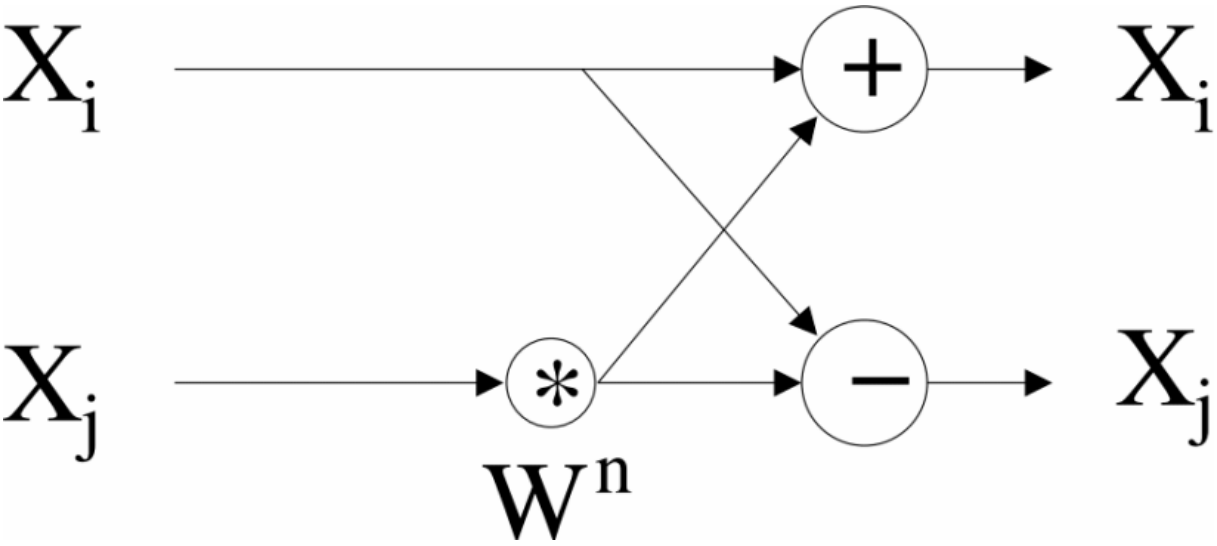

Fig. 8. Description of the BFU operation

Fitter Status	Successful - Sun Jan 09 01:38:05 2011
Quartus II Version	9.1 Build 222 10/21/2009 SJ Full Version
Revision Name	cfft1024X16
Top-level Entity Name	cfft1024X16
Family	Cyclone II
Device	EP2C8Q208C8
Timing Models	Final
Total logic elements	3,162 / 8,256 (38 %)
Total combinational functions	3,014 / 8,256 (37 %)
Dedicated logic registers	2,063 / 8,256 (25 %)
Total registers	2063
Total pins	104 / 138 (75 %)
Total virtual pins	0
Total memory bits	53,248 / 165,888 (32 %)
Embedded Multiplier 9-bit elements	0 / 36 (0 %)
Total PLLs	0 / 2 (0 %)

Fig. 9. Synthesis results of 256-floating point FFT processor

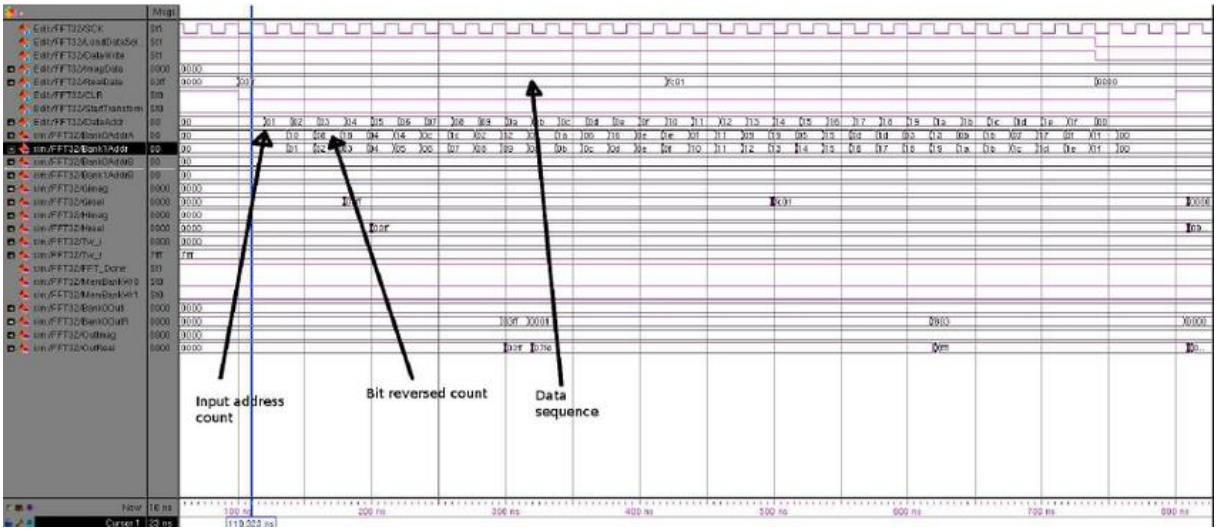

Fig. 10. Waveforms showing sequence of input data.

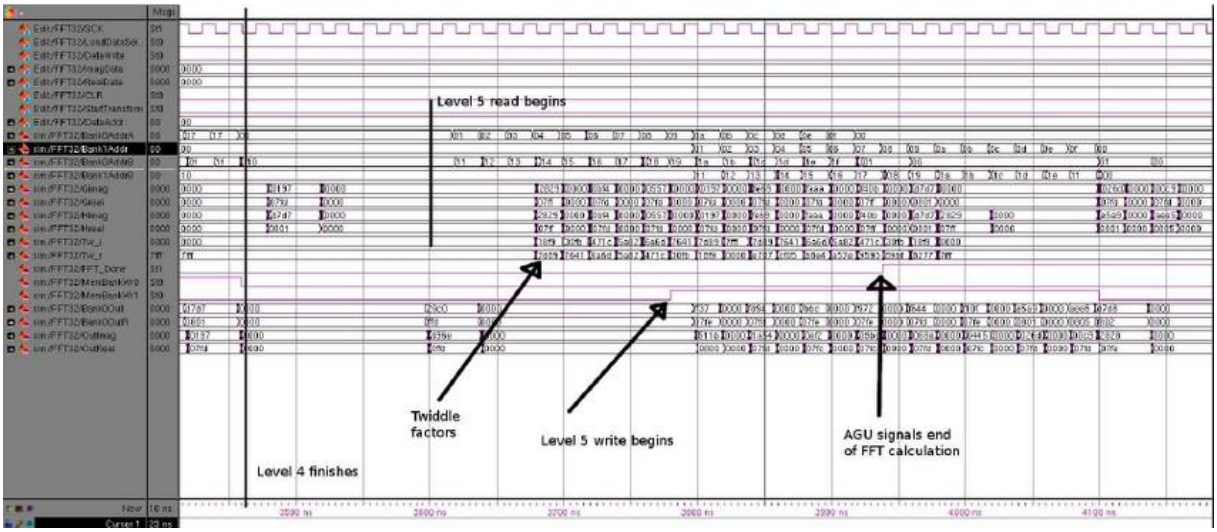

Fig. 11. Final data as it is written to Bank 1 is present in the bottom four waveforms.

3.3 Fault detection module

In the fault-detection module, outputs from the FFT processor are presented to simple comparator to determine if the threshold for a particular harmonic has been exceeded. The floating point comparator is designed using the Altera floating point Megafunction [28]. The MegaWizard Plug-In Manager of Quartus is used to create the design file which is then instantiated in the designed fault detection module. Under variable load conditions of the drive system, the threshold can be adjusted if necessary as a function of load (if IQ current is passed from the controller to the fault detection routine) using an adaptive threshold. The fault decision making algorithm is shown in Fig 12.

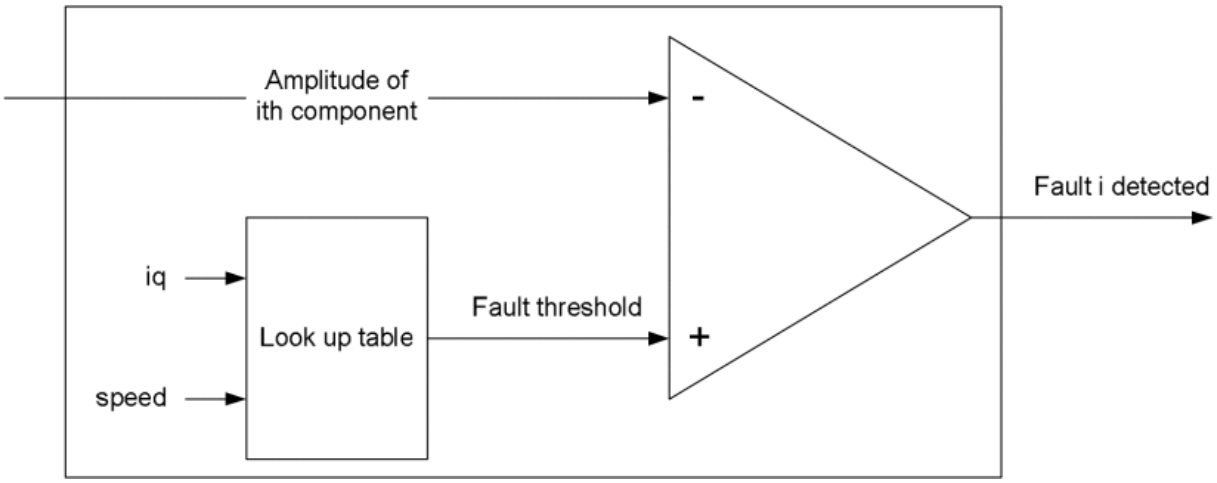

Fig.12. Decision making algorithm

4 Experimental results and analysis

4.1 Experimental test bench

To verify the proposed real-time fault detection algorithm, an experimental test stand was set up as presented in Fig. 13. The test machine is an 8 poles 4.5 kW IPMSM from Leroy Somer operating under FOC-based inverter in speed control mode. The parameters of the machine are given in Table I. In the experiments, the dc bus voltage is set at 50-V. The pulse-width-modulation (PWM) frequency is 5-kHz, the voltage pulse width for the complex phasor estimation procedure is chosen to be equal the PWM period. The motor has been operated at 3% rated speed and no-load. The rotor position is sensed by the absolute encoder with 4096 edges per mechanical revolution (12 bits). All the machine control and fault detection algorithms are implemented in the developed printed circuit board (named MLC Controller) with Cyclone III EPC40 FPGA and Texas Instrument C2000 series microcontroller TMS320F2877s. The main board is responsible for mapping signals from MCU and FPGA to/from converter, measurement probes, etc.

The In-System Memory Content Editor of Quartus was utilized to obtain results in real-time from a RAM designed within FPGA (FFT results from FPGA, complex phasor from DSP, transferred to FPGA) and analysed in Matlab. Fig. 14 shows the real-time acquisition of FFT results from FPGA using the In-System Memory Content Editor.

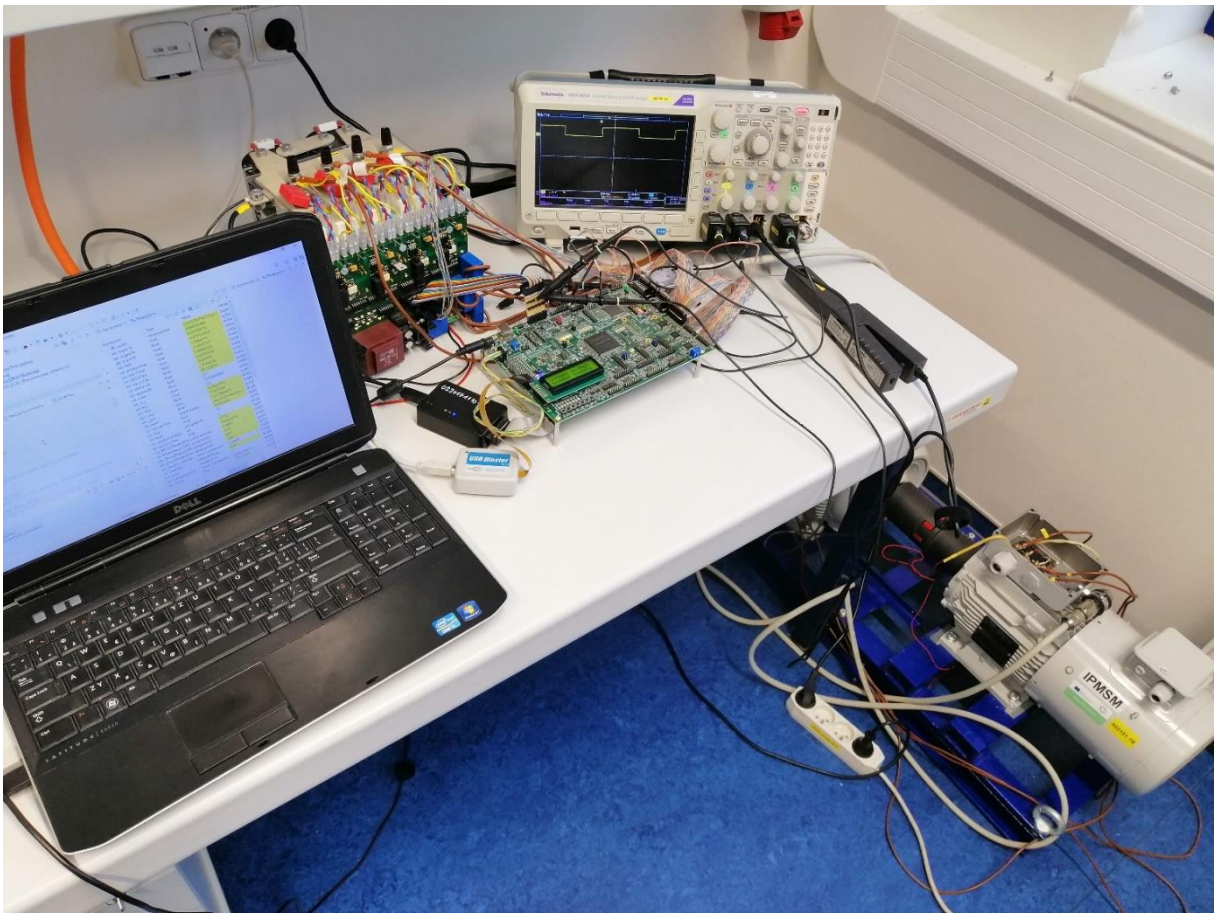

Fig.13. Experimental set up

Parameter	Description	Value
$P_n[kW]$	Nominal power	4.5
$P_p[-]$	Number of pole pairs	4
$\omega_m[RPM]$	Nominal speed	1500
$R_s[\Omega]$	Stator resistance	1.176
$L_s[mH]$	Stator inductance	16
$L_d[mH]$	Stator inductance in d axis	14
$L_q[mH]$	Stator inductance in q axis	19
$\psi_{PM}[Wb]$	Magnetic flux	0.438
$V_{DC}[V]$	DC voltage	50
$f_c[kHz]$	Switching frequency	5
N_s[-]	Number of slots	12

Table. I. Parameters of the machine

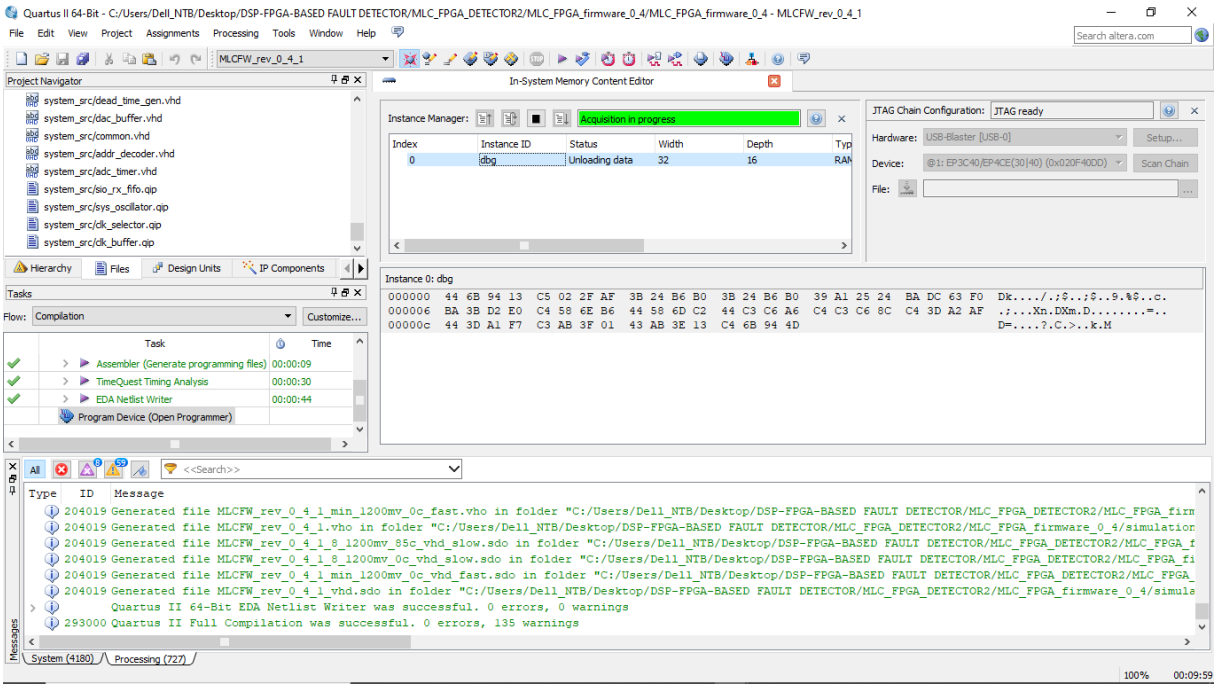

Fig.14. Real-time acquisition of FFT results from FPGA.

4.2 Algorithm testing with open phase fault

To test the proposed algorithm, an open phase fault was simulated as shown in Fig. 15. During the open phase experiment, Rop resistor was inserted into phase leg. The value of the resistance is set to 10 Ohms.

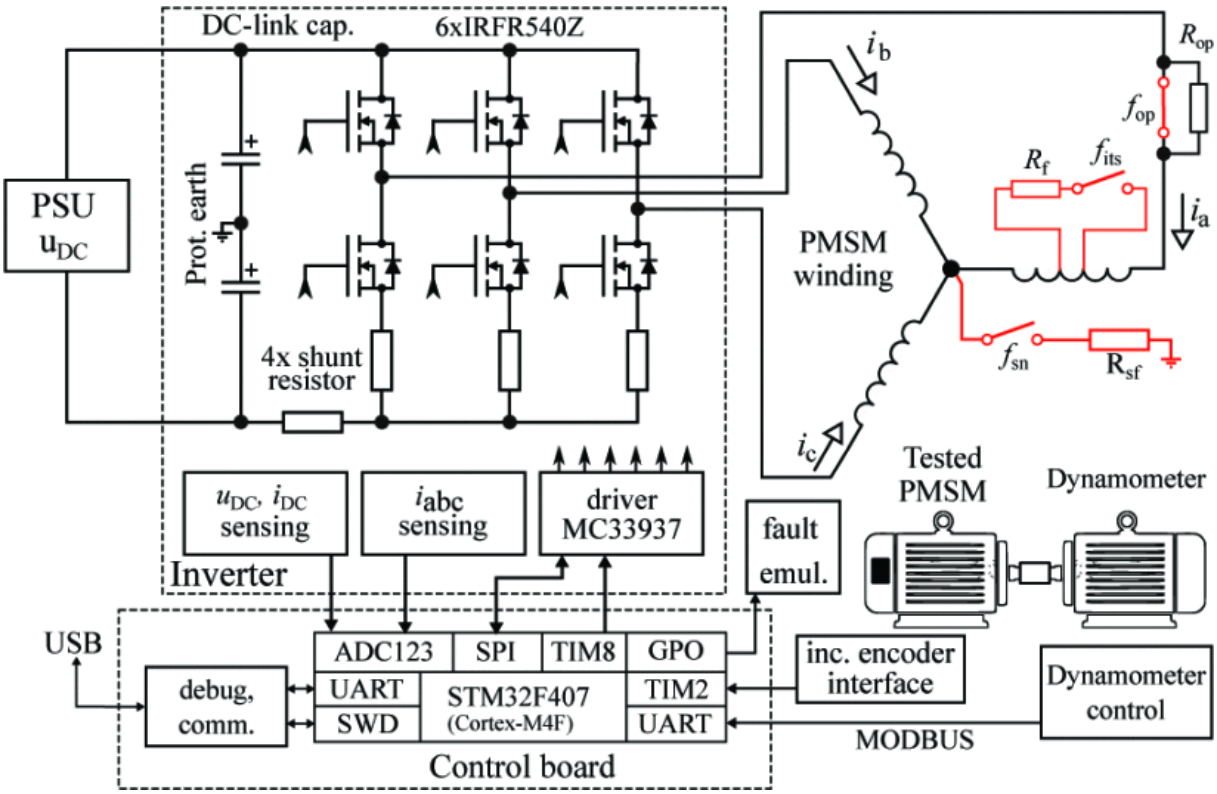

Fig. 15. Block diagram of the considered inverter realization with HW emulated faults (in red colour)

4.3 Detection open phase fault using the complex phasor

In order to use the complex phasor for detection of open phase faults, it is necessary to consider and separate all inherent asymmetry components that are present in standard synchronous electrical machines. As even a symmetrical and faultless machine shows some inherent asymmetries, consequently, there are always some modulations detectable in the asymmetry phasor.

The main asymmetry is the saturation saliency that is caused by the different levels of saturation arising from the fundamental wave along the circumference. It has a modulation period that is equal to twice that of the fundamental wave which corresponds to the machine's number of poles. In addition, the magnitude of the saturation saliency depends on the flux and load level of the machine. Another inherent asymmetry results from the remanent magnetic induction of the permanent magnets. As a source of magnetic flux, the magnets can, evidently, introduce harmonics in the machine's magnetic field. As the magnets rotate at the mechanical speed, evidently the magnets as such do not change in time. The remanent magnetic induction will thus only contain harmonic combinations that rotate at mechanical radians per second. It contain harmonic orders that are a multiple of pole pairs including the fundamental harmonic. Note that this demand requires p identical repetitions of the magnet distribution where p is the number of pole pairs. If, for example, one of the magnets is demagnetized, it is no longer valid. Like the magnets, the winding distribution introduces harmonics in the machine's magnetic field. Due to the distribution of the windings, the induced spatial-harmonic orders have to satisfy this equation [22]: k = p (1+ c*N*m), where k is the kth induced harmonic, N is the number of slot per pole and per phase, m the number of phase of the machine, and c, an integer. The machine's geometry also introduces harmonics in the machine's magnetic field results from the openings of slots in the lamination that cause slotting modulation. It contain harmonic orders that are a multiple of number of slot. Also, the saturation saliency, the magnets, the winding distribution, and the machine's geometry create additional harmonic combinations that depend on the point of operation.

Assuming now a stator related fault (e.g., open-circuit fault, turn-to-turn fault) the electromagnetic properties of the stator winding changes and thus also the transient leakage inductance. Considering now a fault at a certain stator position, this will induce an asymmetry equal to the number of poles when moving the rotor and thus the excitation direction for one full mechanical revolution. As the machine considered has eight poles, the harmonic to track for the open phase fault detection is the eight harmonic. So, a fault induced asymmetry will be detectable in the saturation saliency harmonic and will be denoted as fault indicator.

If machines with pole numbers other than eight are used, the harmonic corresponding to the pole number has to serve as fault indicator instead.

The real and imaginary portion of the complex phasor set signal for a symmetrical machine are given in Figs. 16 and 17, respectively. It can be clearly seen that the signals contain a modulation with a period of 8 corresponding to the spatial period (one mechanical revolution). This modulation correspond to the number of pole of the machine. In the

spectral presentation, all spectra represent the spatial distribution of the transient leakage inductance along the air gap. All the values are given in arbitrary units [a.u.] according to the signal processor internal representation. These arbitrary units are equal to the values used from the digital signal processor (DSP) for quantization according to the ADC values. The harmonic content of the complex phasor is shown in Fig. 20. The horizontal axis of the diagram shows the harmonic number where the fundamental wave corresponds to one mechanical revolution of the rotor. As the asymmetry phasors are complex values the resulting spectrum also is of complex nature. As can be seen, several harmonics are visible in the spectrum caused by the interaction of rotating magnetic flux and remanent magnetic induction of the permanent magnets and also by some parasitic effects of the machine. The signal offset is mainly caused by the remanent magnetic induction of the permanent magnets. The $\pm4^{th}$, $\pm12^{th}$, $\pm16^{th}$, $\pm24^{th}$, harmonic etc., are also create by the magnets as magnets induce harmonic orders that are a multiple of pole pairs. The stator of the present machine has 12 stator slots thus the $\pm12^{th}$ harmonic is related to this parameter. The machine has 8 poles thus, the saturation asymmetry is the $\pm8^{th}$ harmonic shown. The $\pm14^{th}$ harmonic results from a combination of magnetic iron core properties and winding distribution. The $\pm20^{th}$ harmonic results from the harmonic combination of saturation, slotting and magnets.

For the open phase fault, the real and imaginary portion of the complex phasor set signal are also given in Figs. 18 and 19, respectively. It can be seen that the real portion signal does not contain a clear modulation with a period of 8 due to the open phase fault, but the amplitude of the complex phasor is increased. However, the modulation with period of 8 is clear visible in the imaginary portion signal because the open phase fault is created in the phase U, so the fault-induced asymmetry does not affect the imaginary part of the complex phasor. The spectral analysis reveals the impact of the fault-induced asymmetry. As can be seen in Fig. 21, when comparing with the symmetrical spectral, there is a big increase of the harmonic amplitudes including the signal offset, saturation, and harmonic orders caused by the permanent magnets as was expected because of the change of the electromagnetic properties of the stator winding caused by the open phase fault. The biggest change however, as expected, is visible in the -8^{th} harmonic (saturation and open phase) that rises from $4 \cdot 10{-}4$ to $4 \cdot 10{-}3$ by a factor of 10 and now becomes by far the most dominant modulation of the complex phasor. The -12^{th} harmonic almost does not changes. The $+12^{th}$ (slotting) harmonic changes from $2 \cdot 10{-}4$ to $1 \cdot 10{-}3$. The 20^{th} harmonic (intermodulation) changes from 0.02 to .004. The -20^{th} harmonic changes from $2 \cdot 10{-}4$ to $1 \cdot 10{-}3$.

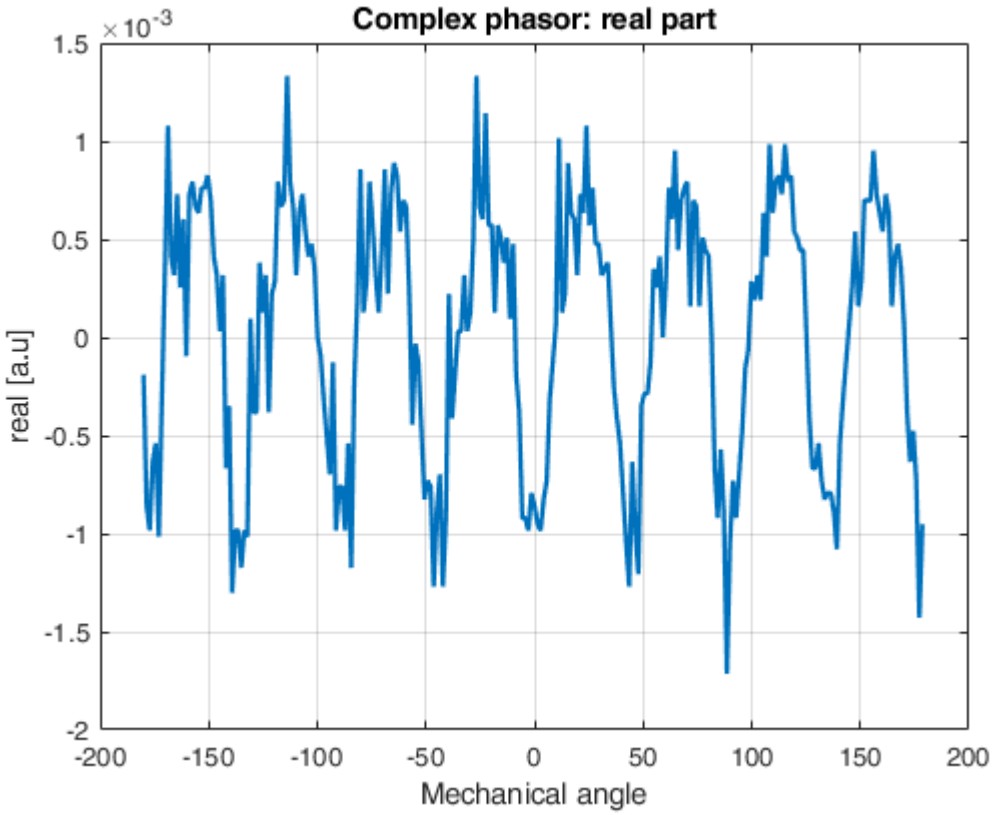

Fig. 16. Real part of the complex phasor set over one mechanical revolution. Machine state: symmetrical.

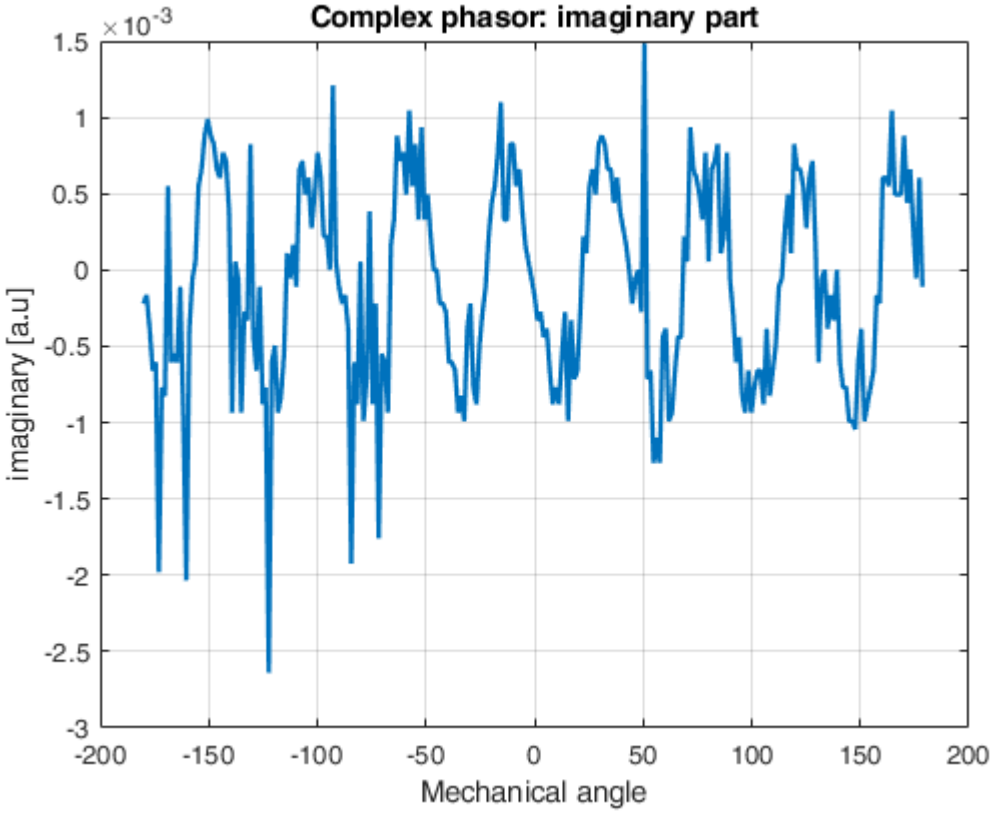

Fig. 17. Imaginary part of the complex phasor set over one mechanical revolution. Machine state: symmetrical.

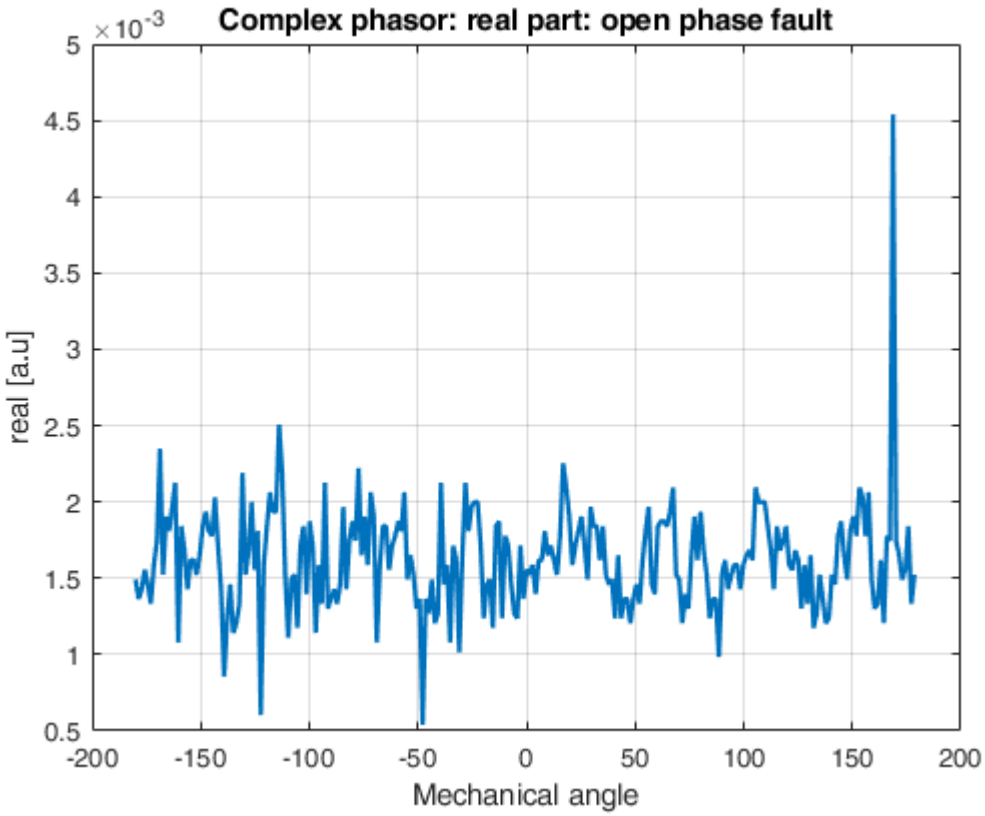

Fig. 18. Real part of the complex phasor set over one mechanical revolution. Machine state: one open phase fault.

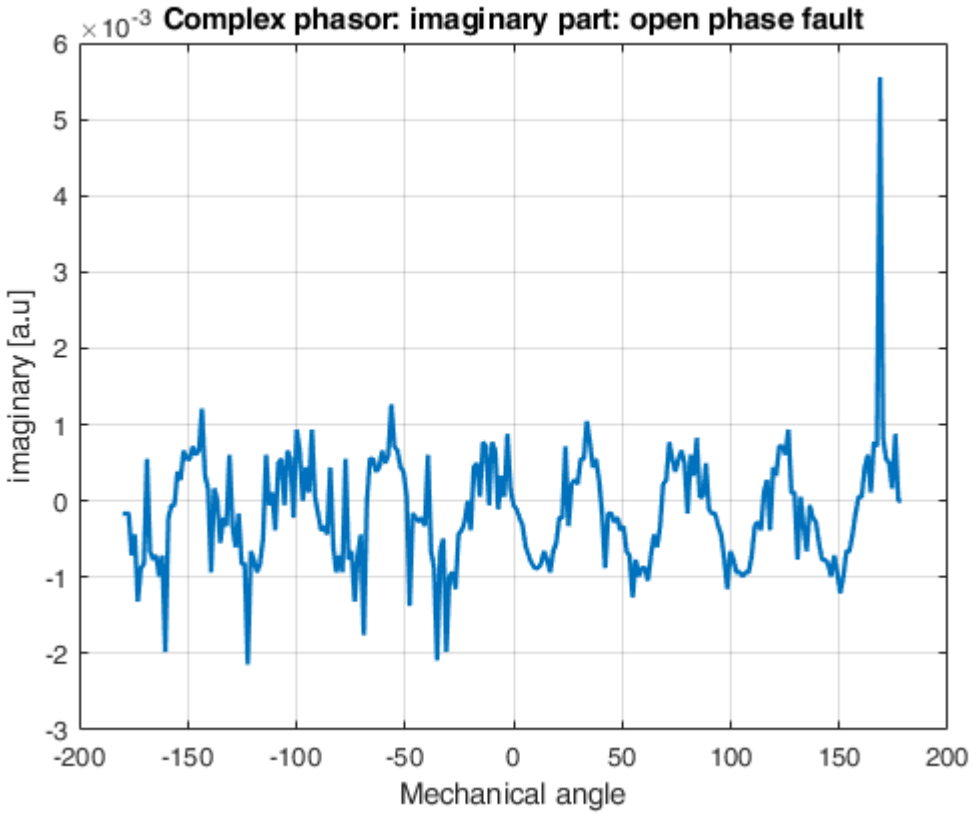

Fig. 19. Imaginary part of the complex phasor set over one mechanical revolution. Machine state: one open phase fault.

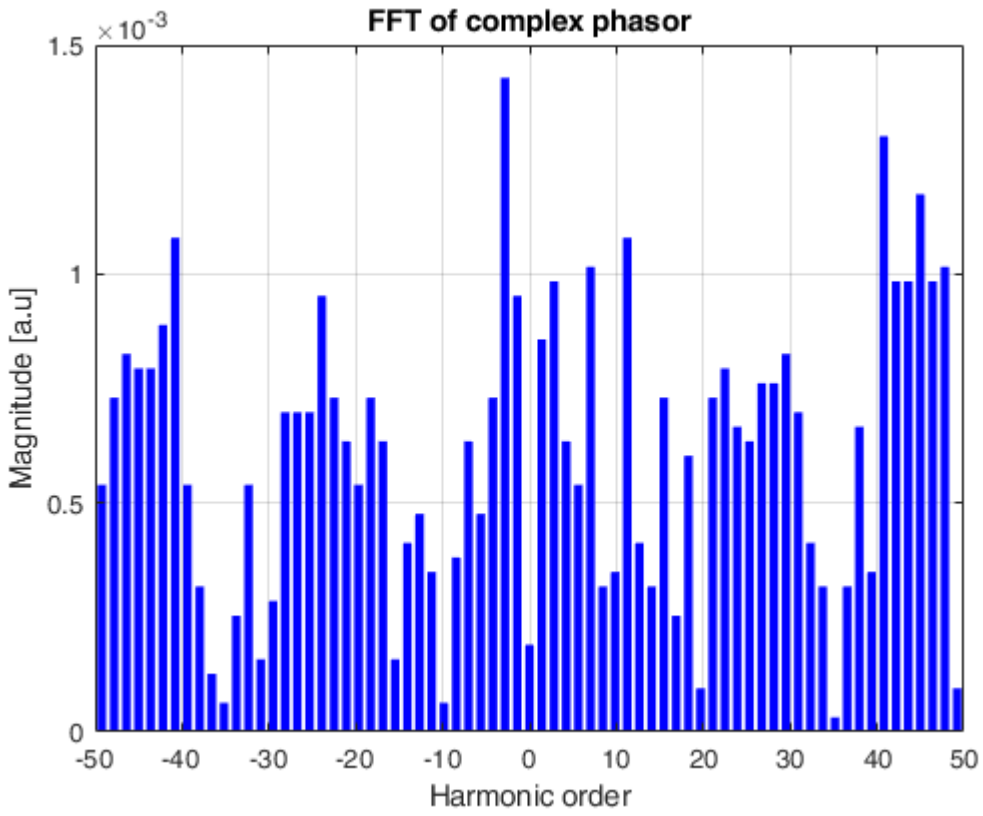

Fig. 20. Harmonic content of the complex phasor of the faultless machine at zero load (horizontal axis: harmonic order scaled to one mechanical revolution).

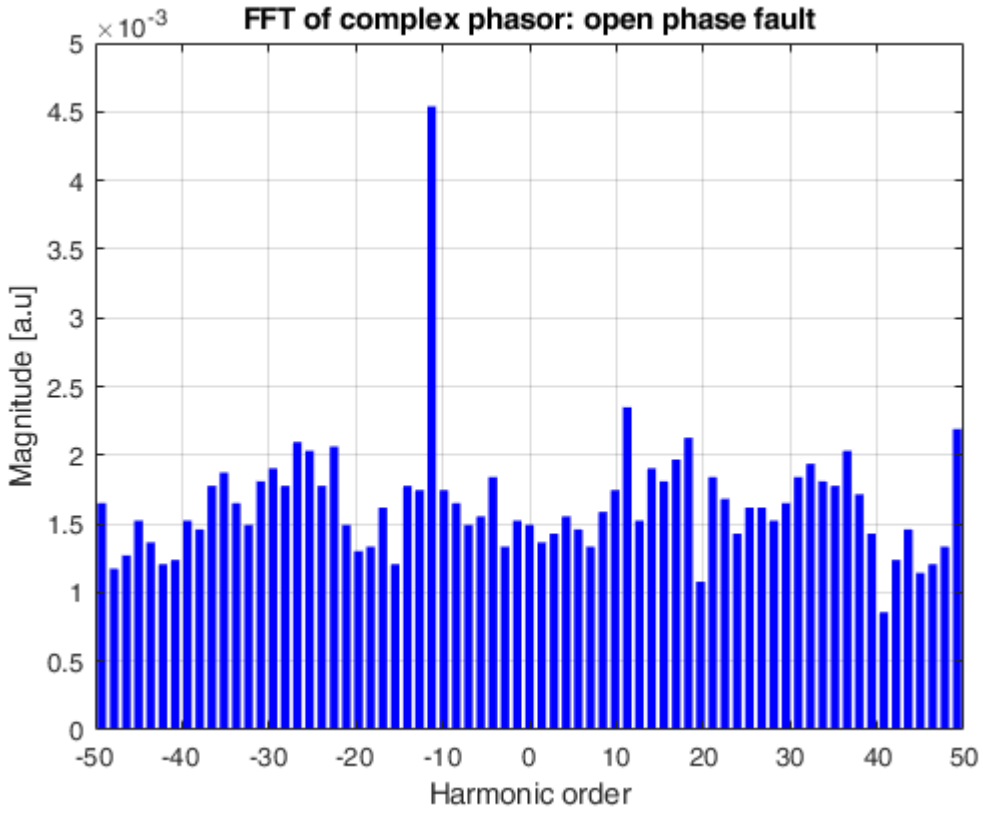

Fig. 21. Harmonic content of the real part of the complex phasor with one open phase fault (horizontal axis: harmonic order scaled to one mechanical revolution; vertical axis: magnitude).

5 Conclusion

The paper has presented a new real-time algorithm for the detection of fault in permanent magnet synchronous motor drive systems, proposed for traction drive applications. The algorithm can be embedded into the drive system and can operate independently of the motor control. The algorithm uses the machine's transient reactance in the frequency domain as condition indicators. This parameter is estimated using an intelligent controller which interrupt the motor control and apply an excitation with voltage pulses using the switching of the inverter and then measuring the resulting current slope. Then a subsequent real-time fast Fourier transform of the obtained values provides indicators to detect faults. The model was implemented in a DSP/FPGA and applicability was verified online on an interior permanent magnet synchronous motor operated by an inverter with zero load. The results have shown a high accuracy of the fault indicator. Future works will be performed when the drive operates at different load levels.

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Revision history

Rev.	Chapter	Description of change	Date	Name
0	All	Document release	15.11.2010	J.Michalík