

Funkční vzorek

Katherine readout for Timepix4



Figure 1. Katherine readout system for Timepix4. The chipboard is connected to the Katherine readout via Ethernet (up to 5 m), while data are transferred to the host computer through either Gigabit Ethernet or an external PCIe Gen3 ×4 interface.

Key features:

- Support up to 8 data lines (2.5Gbps/5 Gbps)
- Data rates:
 - up to 9 MHit/s (Gigabit Ethernet)
 - up to 350 MHit/s (PCIe Gen3 4x)
- Bias source: up to ± 1 kV (covering Si, GaAs, CdTe sensors)
- Low-level data processing in FPGA
- User-friendly control SW (Windows only)

- ▶ V souladu s platnou metodikou Úřadu vlády ČR je uplatňován funkční vzorek.
- ▶ This result was funded by Technology Agency of the Czech Republic, grant number TN02000012/001.

Description:

The Katherine readout device is the core of the acquisition ecosystem for Timepix4-based detectors. Timepix4 detectors are developed within the Medipix Collaboration at CERN and represent state-of-the-art pixel detector technology. The device is designed with a modular architecture consisting of a main detector platform and an interconnectivity board that provides the physical interface to the chipboard (a PCB carrying the Timepix4 detector). The detector platform, based on an SoC FPGA device, implements all key functionalities, including communication with the host computer, signal processing, and readout control. Thanks to this modular approach, the system can be readily adapted to other detector types by replacing only the interconnectivity board. In its current version, the readout device provides two data interfaces: Gigabit Ethernet and PCIe via an external cable. These interfaces offer complementary advantages, enabling both remote control and operation (Ethernet) and high data-rate acquisition (PCIe). The device also integrates a high-voltage bias power supply supporting sensor biasing up to 1 kV. To facilitate integration into experimental setups, several GPIO lines are available for external triggering and clock synchronization.

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